Remarks

The Office Action dated December 5, 2007 indicated that claims 1-15 stand rejected under 35 U.S.C. § 103(a) over Cassetti *et al.* (U.S. Patent No. 6,311,302) and further in view of Nadeau-Dostie *et al.* (U.S. Patent Pub. No. 2002/0184562).

Applicant respectfully traverses the § 103(a) rejection of claims 1-15 because the Office Action fails to cite to any reference that teaches setting a bit in each of a plurality of TAP controllers to a known state and selecting one of the TAP controllers based on the state of each of these bits. Applicant maintains that the cited portions of the Cassetti reference do not teach setting a bit in each of a plurality of TAP controllers to a known state for the reasons presented in the Appeal Brief dated August 29, 2007 which is hereby incorporated in its entirety by reference. For example, the bits relied upon in the rejection are taught to be located in the TLM register (20, 36), which is taught to be external to TAPs 16, 18, 30 and 32. The Office Action does not address this deficiency as Applicant respectfully submits that the cited portions of the Nadeau-Dostie reference also fail to teach generating such a signal from a bit in each of TAP controllers (*e.g.*, 12, 14 and 16). The following description details how the cited portions of Nadeau-Dostie teach a register (*e.g.*, register 32), entirely within master TAP 12, is used to select a TAP controller, rather than a bit in each of the TAP controllers 12, 14 and 16.

The cited portions of Nadeau-Dostie teach setting bits in master TAP 12 and selecting a group of TAPs based on these bits. More specifically the cited portions of Nadeau-Dostie teach that embedded TAPs 14 and 16 are in a first group 22 and the master TAP 12 forms a second group. *See, e.g.,* Figure 1 and Paragraph 0028. The most significant bits of the instruction register of master TAP 12 define a selection code for use in selecting the TAP group whose instruction register and test data registers will be accessed next. *See, e.g.,* Paragraph 0036. Thus, Nadeau-Dostie only sets bits in master TAP 12 in order to select a group of TAPs. There is no bit (or bits) in embedded TAPs 14 and 16 that are set in order to select the group of TAPs. Thus, the Office Action has not shown correspondence to setting a bit in each of a plurality of TAP controllers and selecting one of the TAP controllers based on each of these bits as in the claimed invention. As neither the Cassetti nor the Nadeau-Dostie reference (nor the alleged combination) teaches setting a bit in each of a plurality of TAP controllers to a known

state and selecting one of the TAP controllers based on the state of each of these bits, Applicant submits that any combination which includes these aspects would appear to be improperly based upon hindsight reconstruction using Applicant's disclosure as a template. *See, e.g.,* M.P.E.P. § 2142. Accordingly, the § 103(a) rejection of claims 1-15 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 1-15 because the rejection relies upon illogical assertions of correspondence. For example, in attempting to assert correspondence to the claimed invention, the Office Action relies upon numerous portions of the Cassetti reference relating to internal TLM's that are part of cores 12 and 14. *See, e.g.,* Figure 1. The Office Action then appears to propose that the internal TLM's be replaced with a TAP controller.

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> But, Cassetti et al fails to explicitly teach that a TAP controller could also replace the TLM controller. However, Nadeau-Dostie et al teaches an integrated circuit (e.g., fig. 1), comprising: a plurality of functional blocks (items 24, 22 and 20, fig.1), each functional block having a test access port (TAP, e.g., items 14, 16 and 12, fig. 1).
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Thus, the Office Action combination does not include the part of the Cassetti reference (*i.e.,* the internal TLM's) upon which the majority of the rejection is based. As such, the portion of the rejection that relies upon functionality alleged to be present in the TLM controllers is improper as the asserted combination does not include such a TLM controller due to the replacement of the internal TLM controllers with TAP controllers.

Moreover, the Office Action confusingly switches between reliance upon the master TAP controller of the Nadeau-Dostie reference and the TLM controller(s) of the Casseti reference. For example, the Office Action states "producing a first signal based, at least in part, on the state of the first bit in each of the plurality of TAP controllers and selecting one of the plurality of TLM controllers…" Applicant respectfully submits that if the TLM controller is to be replaced by a TAP controller, as suggested by the Office

Action, selection of the replaced TLM controller is illogical. Accordingly, the § 103(a) rejection of claims 1-15 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 103(a) rejection of claims 1-15 because the Office Action has improperly pieced together portions of different portions of the cited Cassetti reference without showing how these portions work together to arrive at the claimed invention. More specifically, the Office Action cites to various portions of the Cassetti reference as allegedly corresponding to several aspects of the claimed invention. *See, e.g.,* Figure 1, Col. 3:6-19, Col. 6:1-10 and Col. 4:53-65. The Office Action then cites to the Background of the Cassetti reference as supposedly corresponding to aspects of the claimed invention directed to producing a first signal based at least in part on the state of the first bits in the TAP controllers. *See, e.g.,* Col. 2:21-50. As is indicated by the Cassetti reference; however, this portion of the Background is discussing teachings of U.S. Patent Application Ser. No. 09/283,171. *See, e.g.,* Col. 2:30-37. Thus, the Office Action appears to be citing to the teachings of two different references; however, the Office Action has not provided any rationale for combining these references nor shown how such a combination could function. This approach is contrary to the requirements of § 103 and relevant law. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007) ("A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art."). Accordingly, the § 103(a) rejection of claims 1-15 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

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